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10/623,101	07/18/2003	Guillermo Rozas	TRAN-P072	2896

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EXAMINER	
RIZZUTO, KEVIN P	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,101	ROZAS ET AL.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined.

2. Acknowledgement of papers filed: amendment filed on 3/13/06. The papers filed have been placed on record.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objection to the drawings set forth in the previous Office Action. Consequently, this objection has been withdrawn by the examiner.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

New Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. As per claim 1, the limitation "*wherein said portion of said corresponding address is independent of region of said memory unit from which said instruction is fetched*" was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification teaches the exact opposite, that is, that the address that is concatenated *is dependent* on the region of said memory unit from which said instruction is fetched. For instance:

a. "[T]he meaning of an instruction is ***additionally dependent on some or all of the address at which the instruction is stored***" (page 3, lines 18-20).

b. "Figure 1 illustrates an instruction 10, ***a corresponding address 20 at which instruction 10 is stored***, and a plurality of ***concatenations 30 and 40 of a portion of the corresponding address 20 and the instruction 10*** in accordance with an embodiment of the present invention. Rather than increasing an instruction set by increasing the size of the instruction 10, the instruction set is increased ***by utilizing one or more bits from the corresponding address 20 of the instruction 10 in memory***." (Page 3, line 22 to page 4, line 4)

c. "***The corresponding address 20 is provided to memory to access the instruction 10***. The corresponding address 20 has k bits." (Page 4, lines 10-11).

d. "Moreover, a particular bit from the corresponding address 20 can be selected whose value would indicate ***whether the corresponding address 20 was an even address or an odd address***." (Page 4, line 23 to page 5, line 2).

e. "The one or more bits from ***the corresponding address 20 can affect the meaning of the opcode portion 5*** and the portion 7 for register identifiers, an immediate, etc." (Page 4, lines 11-12).

f. "***The compiler 240 generates the plurality of instructions and stores each instruction at an appropriate address in the memory unit 230 to facilitate the concatenation operation that determines the meaning of the instruction***. For example, if an instruction needs to be stored at an even address to obtain a desired meaning, the compiler or translator ensures that it is stored at an even address. The compiler or translator does similar word for other alignments." (Page 4, line 21 to page 5, line 4).

8. As is shown in the above cited portions, said portion of said corresponding address is ***dependent*** on the region of said memory unit from which said instruction is fetched. It is specifically stated that compiler 240 "stores each instruction at an appropriate address in the memory unit 230 to facilitate the concatenation operation that determines the meaning of the instruction." (Page 4, line 21 to page 4, line 1) If "said portion of said corresponding address" was *independent* of the region of said memory unit from which said instruction is fetched, there would be no need for the compiler to store "each instruction at an

appropriate address." Furthermore, by definition, an instruction address indicates what region an instruction is in within a memory, thus, inherently an instruction's address is *dependent* on the instruction's location in memory.

9. Therefore, the newly amended limitation, "wherein said portion of said corresponding address is independent of region of said memory unit from which said instruction is fetched" was not supported or described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor(s), at the time the application was filed, had possession of the claimed invention

10. Given the similarities between claim 1 and claims 5 and 10, the arguments as stated for the rejection of claim 1 also apply to claims 5 and 10.

11. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

12. As per claim 1, the limitation "*wherein said portion of said corresponding address is independent of region of said memory unit from which said instruction is fetched*" was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification teaches the exact opposite, that is, that the address that is concatenated is dependent on the region of said memory unit from which said instruction is fetched. See above cited portions of Applicant's specification (paragraphs a-f above). It is contrary to what is known

in the art to have an instruction address contain address bits that are independent of said instruction's region of memory. The purpose of an instruction address, as is well known in the art, is to point to a region of memory at which said instruction resides. Applicant has claimed, "wherein said portion of said corresponding address is independent of region of said memory unit from which said instruction is fetched", which is contrary to what is known in the art and no description in the specification is found that would enable one skilled in the art to make and/or use the invention.

13. Given the similarities between claim 1 and claims 5 and 10, the arguments as stated for the rejection of claim 1 also apply to claims 5 and 10.

14. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. As per claim 1, the limitation "*wherein said portion of said corresponding address is independent of region of said memory unit from which said instruction is fetched*" is indefinite. It is contrary to what is known in the art to have an instruction address contain address bits that are independent of said instruction's region of memory. The purpose of an instruction address, as is well known in the art, is to point to a region of memory at which said instruction resides. Since it is inherent that an instruction address is dependent on the region of the memory from which said instruction is fetched, it is unclear the metes and bounds of the limitation. From one point of view, it may be that Applicants intent is for the concatenated portion of the address is in fact not an address. Another possibility

is that it is intended to be an address, at which point it is unclear how an address can be independent of said instructions region in memory. Therefore, the limitation "*wherein said portion of said corresponding address is independent of region of said memory unit from which said instruction is fetched*" is indefinite and will not be further treated, as it would be mere speculation by the Examiner as to what the intended meaning of the limitation is.

16. Given the similarities between claim 1 and claims 5 and 10, the arguments as stated for the rejection of claim 1 also apply to claims 5 and 10.

Maintained Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1-3, 5-7 and 10-12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Larson, U.S. Patent 5,115,500.

19. Examiner notes that since the newly amended portions to claims 1, 5 and 10 are new matter, have not been enabled and are indefinite, they have not been given patentable weight and are not addressed below.

20. As per claim 1, Larson teaches a method of processing an instruction, said method comprising:

g. Fetching said instruction using a corresponding address from a memory unit: [An instruction is fetched from the I-Store 2 using an address from the memory unit (Instruction Address Register, IAR 3). (Fig. 2, col. 5, line 34 to col. 6, line 40)]

h. Wherein a plurality of possible meanings are associated with said instruction: [There are a possibility of a plurality of meanings for each instruction depending on the concatenated address bits. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

i. Concatenating a portion of said corresponding address to said instruction to form an extended instruction: [IDSR and IDR is a concatenation of a portion of the address bits and the instruction fetched, which forms an extended instruction. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

j. And executing said extended instruction, wherein said portion of said corresponding address determines a meaning for said extended instruction from said possible meanings: [The instruction is decoded and then executed with one of the possible meanings, which is dependent on the extended instruction formed from the concatenation. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

21. As per claim 2, Larson teaches the method as recited in Claim 1 wherein said portion is an address bit. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

22. As per claim 3, Larson teaches the method as recited in Claim 1 wherein said portion is a plurality of address bits. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

23. As per claim 5, Larson teaches a method of handling an instruction, said method comprising:

k. Generating said instruction, wherein a plurality of possible meanings are associated with said instruction: [Instructions reside in the I-Store 2 (fig. 2), there are present, therefore they were inherently generated. Each instruction has a plurality of meanings associated with it, dependent on the corresponding address at which it is stored. (Col. 3, lines 15-22, and col. 5, line 34 to col. 6, line 40.)]

l. Storing said instruction at a particular address in a memory unit such that a portion of said particular address enables determination of a meaning for said instruction from said possible meanings: [Fig. 2, col. 2, lines 21-54 and col. 5, line 34 to col. 6, line 40.]

m. And before executing said instruction, fetching said instruction using said particular address from am memory unit and concatenating said portion of said particular address to said instruction: [Fig. 2, col. 3, lines 52-64 and col. 5, line 34 to col. 6, line 40.]

24. As per claim 6, given the similarities between claim 6 and claim 2, the arguments as stated for the rejection of claim 6 also apply to claim 2.

25. As per claim 7, given the similarities between claim 7 and claim 3, the arguments as stated for the rejection of claim 7 also apply to claim 3.

26. As per claim 10, given the similarities between claim 10 and claim 1, the arguments as stated for the rejection of claim 10 also apply to claim 1.

27. As per claim 11, given the similarities between claim 11 and claim 2, the arguments as stated for the rejection of claim 2 also apply to claim 11.

28. As per claim 12, given the similarities between claim 12 and claim 3, the arguments as stated for the rejection of claim 3 also apply to claim 12.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 4, 8-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson, U.S. Patent 5,115,500.

31. As per claim 4, Larson teaches the method as recited in Claim 1 wherein said plurality of possible meanings are specified by the extended instruction. However, Larson fails to teach specific examples of instructions, the invention is taught with generic examples, such as "type 1" and "type 2" instructions, but does not state what functions the instructions specifically perform. Therefore, Larson fails to teach wherein the plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

32. However, Examiner takes Official Notice that integer type and floating point type instructions are well known in the art and required by many programs

and are present in the vast majority of instructions, and therefore are included in machine languages and capable of being executed by processors.

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made to decode some instructions as integer and floating point instructions, and in the system of Larson, this would inherently mean the address is used to give the integer or floating point instruction this meaning out of a plurality of possible meanings, since Examiner takes Official Notice integer and floating point instructions are well known instructions in instruction sets.

34. As per claim 8, given the similarities between claim 8 and claim 4, the arguments as stated for the rejection of claim 4 also apply to claim 8.

35. As per claim 13, given the similarities between claim 13 and claim 4, the arguments as stated for the rejection of claim 4 also apply to claim 13.

36. As per claim 9, Larson is silent on specifically how the instructions are generated and stored in the memory in the specific locations. While Larson describes that high-level programs are compiled before inherently being placed in an instruction memory for execution (Col. 1, lines 11-29), and that the instructions are stored in specific locations so as to define the decoding of the instructions, Larson does not specifically state that the I-Store 2 contains instructions compiled from high-level code, which were generated and stored by use of the compiler. Therefore, while Larson teaches all the actions taken by the compiler, that is, the instructions are generated and stored at specific locations, Larson fails to teach a compiler performs these actions.

37. However, Examiner takes Official Notice that compilers are used to generate and store instructions in memory, so as to allow programmers to write code in high level languages and allow the compiler to convert and prepare the code for execution by a processor.

38. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the generating and storing of the instructions using a compiler since Examiner takes Official Notice compilers are well known in the art and allow programmers to write code in high-level languages instead of machine code.

39. As per claim 14, given the similarities between claim 14 and claim 9, the arguments as stated for the rejection of claim 9 also apply to claim 14.

Response to Arguments

40. Applicants arguments filed on 3/13/06 have been fully considered but they are not persuasive.

41. Applicant argues the novelty/rejection of claims 1, 5 and 10.

"However, Larsen fails to show concatenating a portion of the corresponding address to the instruction to form an extended instruction, wherein the portion of the corresponding address is independent of region of the memory unit from which the instruction is fetched, as in the invention of independent claim 1.""

42. These arguments are not found persuasive for the following reasons:

n. To clarify, applicant's attention is directed towards the 35 U.S.C. 112 Rejections found above. The added limitation, "said corresponding address is independent of region of said memory unit from which said

instruction is fetched", is indefinite, lacks enablement and is new matter, therefore, the limitation has not been addressed and the previously set forth 35 U.S.C. 102 Rejections and 35 U.S.C. 103 Rejections have been maintained.

Conclusion

43. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

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